

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
2 a circuit configured to receive an input clock signal and to generate an
3 output phase at a predetermined time relative to said input clock signal and
4 dependent on a logic phase width of said input clock signal.
- 1 2. The apparatus as in claim 1, wherein said predetermined time is relative
2 to at least one of a rising edge of said input clock signal, and a falling edge of
3 said input clock signal.
- 1 3. The apparatus as in claim 1, wherein said circuit includes similar circuit
2 components and dissimilar circuit components;
3 wherein at least two of said similar circuit component units are unequal;
4 and
5 wherein said predetermined time is further dependent on the units ratio of at
6 least two similar circuit components.
- 1 4. The apparatus as in claim 1, wherein said circuit is further configured to
2 provide a first signal and a second signal, compare said first signal and said
3 second signal, and generate said output phase dependent on said comparison
4 of said first signal and said second signal.
- 1 5. The apparatus as in claim 4, wherein said comparison is provided by a
2 comparator.
- 1 6. The apparatus as in claim 1, wherein said apparatus is cascaded with at
2 least one reproduction of said apparatus, and configured to provide a multiple
3 of said input clock signal.
- 1 7. The apparatus as in claim 1, wherein said apparatus is coupled in
2 parallel with at least one reproduction of said apparatus, and configured to
3 provide at least two of said output phase generated in parallel during said input
4 clock signal.

- 1 8. A method comprising:
2 receiving an input clock signal and generating an output phase at a
3 predetermined time relative to said input clock signal and dependent on a logic
4 phase width of said input clock signal.
- 1 9. The method as in claim 8, wherein said predetermined time is relative to
2 at least one of a rising edge of said input clock signal, and a falling edge of said
3 input clock signal.
- 1 10. The method as in claim 8, wherein said method includes using similar
2 circuit components and dissimilar circuit components;
3 wherein at least two of said similar circuit components units are unequal;
4 and
5 wherein said predetermined time is further dependent on the units ratio of at
6 least two similar circuit components.
- 1 11. The method as in claim 8, further comprising providing a first signal and
2 a second signal, comparing said first signal and said second signal, and
3 generating said output phase dependent on said comparison of said first signal
4 and said second signal.
- 1 12. The method as in claim 8, further providing a multiple of said input clock
2 signal.
- 1 13. The method as in claim 8, further providing a multiple of said input clock
2 signal.
- 1 14. A chipset comprising:
2 an embedded circuit block including a circuit configured to receive an
3 input clock signal and to generate an output phase at a predetermined time
4 relative to said input clock signal and dependent on a logic phase width of said
5 input clock signal.
- 1 15. The chipset as in claim 14, wherein said predetermined time is relative
2 to at least one of a rising edge of said input clock signal, and a falling edge of
3 said input clock signal.

3 wherein at least two of said similar circuit components units are unequal;
4 and
5 wherein said predetermined time is further dependent on the units ratio of at
6 least two similar circuit components.

1 24. The chipset as in claim 21, wherein said embedded circuit block further
2 comprising means for providing a first signal and a second signal, comparing
3 said first signal and said second signal, and generating said output phase
4 dependent on said comparison of said first signal and said second signal.

1 25. The chipset as in claim 21, said embedded circuit block further
2 comprising means for providing a multiple of said input clock signal.

1 26. The chipset as in claim 21, said embedded circuit block further
2 comprising means for providing at least two of said output phase generated in
3 parallel during said input clock signal.